

Appl. No. 10/733,626  
Examiner: Nhu, David, Art Unit 2818  
In response to the Office Action dated April 4, 2005

Date: July 3, 2005  
Attorney Docket No. 10113421

#### **AMENDMENTS TO THE SPECIFICATION**

Please replace the paragraph at page 3, line 12 with the following amended paragraph:

-- The method of fabricating memory cells of the stacked gate flash memory device in accordance with the present invention comprises providing a substrate, forming a plurality of parallel long trenches along a first direction in the substrate, forming a conductive layer and a pair of source regions on the bottom of each long trench, wherein the source regions are respectively disposed in the substrate adjacent to two sidewalls of each long trench and electrically connected to the conductive layer, forming a source isolation layer on each conductive layer, forming a tunnel oxide layer on two sidewalls of each long trench, contacting the source region thereby, forming a pair of floating gates on the source isolation layer, respectively contacting the tunnel oxide layer, forming a pair of inter-gate dielectric layers, respectively overlying the floating gate, forming a pair of control gates, respectively overlying the inter-gate dielectric layer, forming a second an insulating layer in each long trench, isolating the control gates, forming a plurality of parallel shallow trench isolation (STI) regions along a second direction, defining a plurality of cell trenches and forming a drain region in the substrate adjacent to each cell trench.